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EXAMINER	
SONG, JASMINE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/444,173	PONG, FONG	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 06/10/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to Amendment filed on 06/10/2004, claim 6 has been canceled by previous amendment, therefor, claims 1-5,7-23 are still pending. All rejections and objections not explicitly repeated below are withdrawn.

Claim Objections

2. Claim 19 is objected to because of the following informalities: *

In claim 19, lines 18, "the processors memory having invalid" should be change to -- the processors and memory having invalid--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1,9 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Jim Handy, the Cache memory book published in 1993 by Academic Press, Inc.

Regarding claim 1, Jim Handy (the author of the cache memory book) teaches the MOESI protocol at page 169 to 172 and table 4.3. This discloses a method for

accessing memory in a multiprocessor system said multiprocessor system including processors and a memory, said method comprising:

Storing data in one or more of a plurality of the processors and the memory (at the beginning, the cache line is Invalid state, the responding processor needs to read certain data, in this case, there is a read miss occurs under the invalid state from CPU bus, the responding processor's cache will be updated from main memory and update status to shared, and the same thing happens when the requesting processor's cache requests the same data, therefore, both processor's cache have the shared state and same data);

In one of the one or more of said plurality of processors where the data is stored, modifying the data (when the responding processor wants to modify (write) the data, there is a write hit under the shared state from the CPU bus, therefore, the responding processor writes to cache line, writes to system bus and update status to Exclusive, then, when the responding processor writes to cache line again, it updates status of the cache line to Modified. Modified state is **Valid** and written to **more than once** by this CPU but unsnooped; page 169, section 4.3.3, first paragraph, see table 4.3);

In the one of the one or more of said plurality of processors that modified the data, associating the modified data with state information indicating that the modified data is valid (Modify state is **Valid** and written to more than once by this CPU but unsnooped);

In the others of the plurality of processors and said memory where the data is stored, associating the data with state information indicating that the data is invalid

(when the other processor snoops the system bus and got the write hit under the shared state, therefore, update status to Invalid; see table 4.3);

From a requesting processor, issuing a request for the modified data to one or more other processors and memory (when the requesting processor wants to issue a request, there is a read miss under the invalid state from the CPU bus, therefore, the requesting processor's cache tries to access main memory and change the processor's cache status to Shared, table 4.3);

In each of the processors and memory that receive the request, checking to determine whether a stored copy of the data valid or invalid (it is taught as the responding processor snoops on the system bus and checks for valid data that hits the snoop);

In the processor having the valid copy of the data, responding to the request and returning the valid copy of the requested data to the requesting processor (when the responding processor wants to respond the request, there is read hit under the Modified state from the system bus, therefore, Disable main memory response, output requested data which is direct data intervention as explained in page 153, starting from lines 3, table 4.3);

In the processors and memory that have invalid copies of the data, dropping the request without responding to the request (the other processors which have invalid data have the read miss under Invalid state from the system bus, therefore, no response occurs as shown in table 4.3).

Regarding claims 9 and 19, Jim Handy (the author of the cache memory book) teaches the MOESI protocol at page 169 to 172 and table 4.3. This discloses a multiprocessor system comprising:

Two or more processors, each in communication with a shared memory (it is taught as main memory) via a memory controller (it is in inherent to have the memory control in the multiprocessors system in order to control the data from shared memory to the processor' cache as taught in the table 4.3);

Said two or more processors and said memory being operable to store data (at the beginning, the cache line is Invalid state, the responding processor needs to read certain data, in this case, there is a read miss occurs under the invalid state from CPU bus, the responding processor's cache will be updated from main memory and update status to shared, and the same thing happens when the requesting processor's cache requests the same data, therefore, both processor's cache have the shared state and same data) and modify data (when the responding processor wants to modify (write) the data, there is a write hit under the shared state from the CPU bus, therefore, the responding processor writes to cache line, writes to system bus and update status to Exclusive, then, when the responding processor writes to cache line again, it updates status of the cache line to Modified. Modified state is **Valid** and written to **more than once** by this CPU but unsnooped; page 169, section 4.3.3, first paragraph, see table 4.3);

When one of said two or more processors modifies the stored data, the one of said two or more processors that modified the data being operable to associate the

modified data with state information indicating that the modified data is valid (Modify state is **Valid** and written to more than once by this CPU but unsnooped); and the others of said two or more processors and said memory that did not modify the stored data being operable to associate the modified data with state information indicating that the stored data is invalid (when the other processor snoops the system bus and got the write hit under the shared state, therefore, update status to Invalid; see table 4.3);

Each of the two or more processors being in communication with the memory controller for issuing a request for the modified data to the others of the two or more processors and said memory (when the requesting processor wants to issue a request, there is a read miss under the invalid state from the CPU bus, therefore, the requesting processor's cache tries to access main memory and change the processor's cache status to Shared, table 4.3);

When one of the two or more processors issues a request for the modified data, each of the two or more processors and the memory that receives the request being operable to check itself to determine whether a stored copy of the data is valid or invalid (it is taught as the responding processor snoops on the system bus and checks for valid data that hits the snoop);

Wherein the one of said two or more processors that modified the data is configured to respond to the request and return the valid copy of the modified data to the one of the two or more processors or memory that issued the request (when the responding processor wants to respond the request, there is read hit under the Modified state from the system bus, therefore, Disable main memory response, output requested

data which is direct data intervention as explained in page 153, starting from lines 3, table 4.3);

the processors and memory having invalid copies of the data are configured to drop the request without responding to the request (the other processors which have invalid data have the read miss under Invalid state from the system bus, therefore, no response occurs as shown in table 4.3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5,7-8,10-18 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jim Handy in view of Van Doren et al., U.S. Patent 6209,065 B1.

Jim Handy teaches the claimed invention as shown above claims 1,9 and 19, Jim Handy does not clearly show that each of the processors communicates with the memory via a memory controller and each of the processors has a point-to-point link with the memory controller for issuing a request for a block of data to the memory controller.

However, Van Doren teaches that each of the processors (Fig.1, element 102-108) communicates with the memory (Fig.1, element 150) via a memory controller

(Fig.1, element 200) and each of the processors has a point-to-point link (Fig.2) with the memory controller for issuing a request for a block of data (Fig.1, col. 5, lines 39-42 and Fig.2, col.7, lines 48-50) to the memory controller (Fig.1, element 200).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Van Doren such as each of the processors has a point-to-point link with the memory controller for issuing a request for a block of data to the memory controller within the multiprocessing systems because each processor can access any data item without a programmer having to worry about where the data is or how to obtain its value in a shared memory system, this frees the programmer to focus on program development (col.1, lines 22-31).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claims 3 and 11, Van Doren teaches each point-to-point link includes two dedicated and unidirectional links (Fig.2, col.7, lines 31-35).

Regarding claims 4 and 12, Van Doren teaches the point-to-point links are control links for sending and receiving requests for blocks of data (Fig. 2, col.7, lines 35-39).

Regarding claims 5 and 13, Van Doren teaches each of the processors has a control path point-to-point link for sending and receiving requests for blocks of data (Fig. 2, col.7, lines 35-39), and a data path point-to-point link for sending and receiving blocks of data (Fig. 2, four data paths connected between shared memory and processors).

Regarding claim 7, Van Doren teaches tracking an identification of a processor that currently has a data block (col.6, lines 20-23); and in response to a cache miss in a requesting processor, using the identification to specifically target a read request to the processor that currently has the requested data block (col.6, lines 57 to col.7, lines 7).

Regarding claim 8, Van Doren teaches maintaining a directory indicating the one or more processors that have a copy of a block of data (Fig.1, element 160); when the block of data is modified, using the directory to issue a write invalidation or write update only to the processors that have the copy of the block of data (col.6, lines 15-20).

Regarding claims 14,15 and 16, Van Doren teaches a directory indicating which processors have a copy of a data block (Fig.1, element 160); wherein the processors are in communication with the directory to identify which other processors have a copy of the data block, and directing requests for the data block only to processors that have a copy of the data block (col.6, lines 20-25 and col.6, lines 66 to col.7, lines 21).

Regarding claim 17, Van Doren teaches the memory controller (Fig.2, element 200) is in communication with a shared cache (Fig.2, element 160), separate from caches of the processors (Fig.1), for buffering most frequently accessed data block (col.6, lines 31-41).

Regarding claims 18, Van Doren teaches each block has state information indicating which processor currently has a valid copy of a data block, and wherein the processors utilize the state information to specially address a processor having the valid copy in response to a cache miss in a requesting processor (col.6, lines 20-25).

Regarding claim 20, Van Doren teaches each of the processors and the shared memory is in communication with a control path interconnect (Fig.1 and Fig.2, the four arrows between shared memory and four processors), and each of the processors is in communication with the control path interconnect via a point-to point link for receiving and sending requests for blocks of data (Fig.1 and Fig.2; col.7, lines 31-42);

each of the processors having a corresponding request queue connecting the point-to-point link of the processor to the control path interconnect (Fig.2), and each of the processors having a corresponding snoop queue (Fig.2, element 222-230) connecting the point-to-point link of the processor to the control path interconnect (Fig.2, col.7, lines 31-42);

the request queue (Fig.2, element 212-220) in communication with a corresponding processor for buffering requests for blocks of data by the processor and

issuing the requests to other processors via the control path interconnect (col.7, lines 31-42); and

the snoop queue (Fig.2, element 222-230) in communication with a corresponding processor for buffering requests for blocks of data destined for the processor (col.7, lines 31-42).

Regarding claims 21 and 22-23, Van Doren teaches that the processor or the shared memory responding to the request is configured to respond to the request asynchronously. This limitation is taught as the processor or the shared memory responding to the request is out of order (col.5, lines 63-67 and col.7, lines 63-65).

Response to applicant's Arguments

7. Applicant's arguments with respect to claims, 1,9 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Mano Padmanabhan 9/20/04

Jasmine Song
Patent Examiner
September 20, 2004

Mano Padmanabhan
Supervisory Patent Examiner
Technology Center 2100

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER